ARC 2019

INTERNATIONAL SYMPOSIUM ON
APPLIED RECONFIGURABLE COMPUTING

Tuesday, 2019-04-09

From	To	Event
08:00	09:00	Registration and Welcome
09:00	09:15	Conference Opening
09:15	10:15	Keynote 1 - Agile Hardware Development with Functional Programming
10:15	10:45	Coffee Break
10:45	12:15	Session 1 - Applications
12:15	13:30	Lunch
13:30	14:00	Session 2 - Partial Reconfiguration
14:00	15:00	Lightning Talks for all Poster Presentations
15:00	15:30	Poster Session and Coffee Break
15:30	17:00	Session 3 - Image and Video Processing
17:00	19:30	Social 1 - Visit to GSI Helmholtz

Wednesday, 2019-04-10

From	To	Event
08:00	09:00	Registration and Welcome
09:00	10:00	Keynote 2 - The Challenges of FPGA Development and Methodologies to Cut Total Cost of Ownership.
10:00	10:30	Coffee Break
10:30	12:00	Session 4 - High-Level Synthesis
12:00	13:15	Lunch
13:15	14:45	Session 5 - CGRAs and Vector Processing
14:45	15:15	Poster Session and Coffee Break
15:15	16:15	Session 6 - Design Frameworks and Methodology
16:15	16:45	Invited Talk - Third Party CAD Tools for FPGA Design — A Survey of the Current Landscape
16:45	22:30	Social 2 - Visit to ESOC and Dinner

Thursday, 2019-04-11

From	To	Event
08:00	09:00	Registration and Welcome
09:00	10:00	Session 7 - Safety and Security
10:00	10:30	Coffee Break
10:30	12:00	Session 8 - Convolutional Neural Networks
12:00	12:15	Conference Closing
12:15	13:15	Lunch
13:15	17:15	TaPaSCo Tutorial

Proceedings

Program

Applications: Fault-Tolerant Architecture for On-Board Dual-Core Synthetic-Aperture Radar Imaging *Helena Cruz, Rui Policarpo Duarte, Horácio Neto*

Optimizing CNN-based Hyperspectral Image Classification on FPGAs *Shuanglong Liu, Ringo S.W. Chu, Xiwei Wang, Wayne Luk*

Supporting Columnar In-Memory Formats on FPGA: The Hardware Design of Fletcher for Apache Arrow *Johan Peltenburg, Jeroen van Straten, Matthijs Brobbel, H. Peter Hofstee, Zaid Al-Ars*

Partial Reconfiguration: Probabilistic Performance Modelling when using Partial Reconfiguration to Accelerate Streaming Applications with Non-Deterministic Task Scheduling *Bruno da Silva, An Braeken, Abdellah Touhafi*

Image and Video Processing: HiFlipVX: an Open Source High-Level Synthesis FPGA Library for Image Processing *Lester Kalms, Ariel Podlubne, Diana Göhringer*

Real-time FPGA implementation of connected component labelling for a 4K video stream *Piotr Ciarach, Marcin Kowalczyk, Dominika Przewlocka, Tomasz Kryjak*

A Scalable FPGA-based Architecture for Depth Estimation in SLAM *Konstantinos Boikos, Christos-Savvas Bouganis*

High-Level Synthesis: Evaluating LULESH Kernels on OpenCL FPGA *Zheming Jin, Hal Finkel*

The TaPaSCo Open-Source Toolflow for the Automated Composition of Task-Based Parallel Reconfigurable Computing Systems *Jens Korinth, Jaco Hofmann, Carsten Heinz, Andreas Koch*

Graph-based Code Restructuring Targeting HLS for FPGAs *Afonso Canas Ferreira, Joao M.P. Cardoso*

CGRAs and Vector Processing: UltraSynth: Integration of a CGRA into a Control Engineering Environment *Dennis Wolf, Tajas Ruschke, Christian Hochberger, Andreas Engel, Andreas Koch*

Exploiting reconfigurable vector processing for energy-efficient computation in 3D-stacked memories *Joao Paulo C. de Lima, Paulo C. Santos, Rafael F. de Moura, Marco A.Z. Alves, Antonio C.S. Beck, Luigi Carro*

Automatic Toolflow for VCGRA Generation to Enable CGRA Evaluation for Arithmetic Algorithms *André Werner, Florian Fricke, Keyvan Shahin, Florian Werner, Michael Hübner*

Design Frameworks and Methodology: Hybrid Prototyping for Many-core Design and Validation *Leonard Masing, Fabian Lesniak, Jürgen Becker*

Evaluation of FPGA Partitioning Schemes for Time and Space Sharing of Heterogeneous Tasks *Umar Ibrahim Minhas, Roger Woods, Georgios Karakonstantis*

Safety and Security: Leveraging the Partial Reconfiguration Capability of FPGAs for Processor-Based Fail-Operational Systems *Tobias Dörr, Timo Sandmann, Florian Schade, Falco K. Bapp, Jürgen Becker*

(ReCo)Fuse Your PRC or Lose Security: Finally Reliable Reconfiguration-based Countermeasures on FPGAs *Kenneth Schmitz, Buse Ustaoglu, Daniel Große, Rolf Drechsler*

Convolutional Neural Networks: Filter-wise Pruning Approach to FPGA Implementation of Fully Convolutional Network for Semantic Segmentation *Masayuki Shimoda, Youki Sada, Hiroki Nakahara*

Exploring Data Size to Run Convolutional Neural Networks in Low Density FPGAs *Ana Goncalves, Tiago Peres, Mário Véstias*

Faster Convolutional Neural Networks in Low Density FPGAs using Block Pruning *Tiago Peres, Ana Goncalves, Mário Véstias*